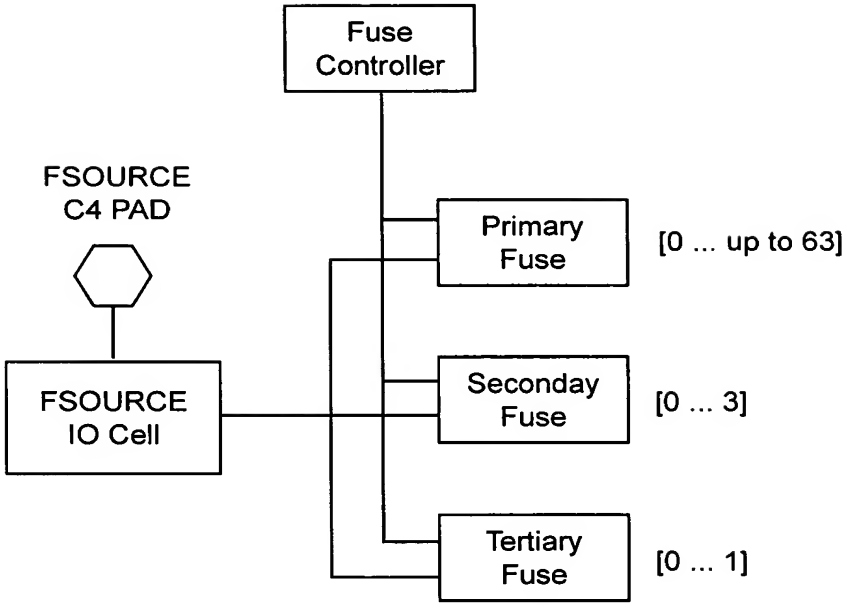


*Figure 1*

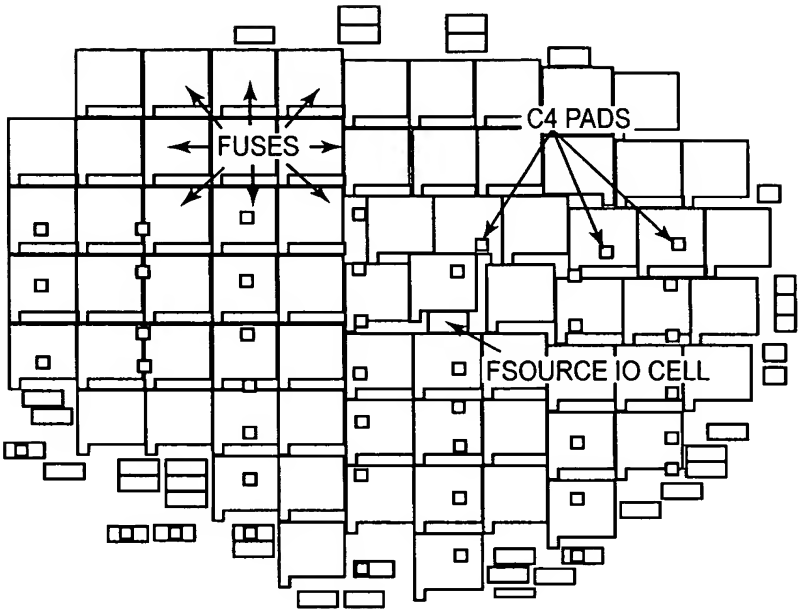


*Figure 2*

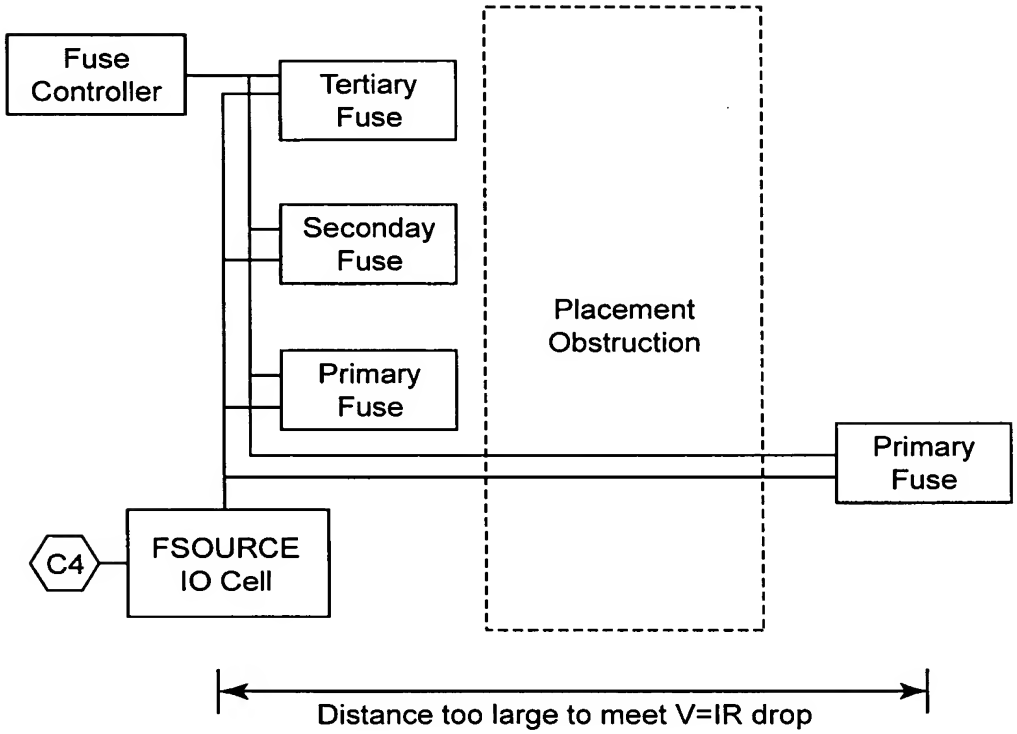
Fuse Controller
Tertiary Fuse
Seconday Fuse
Primary Fuse
Placement Obstruction
Primary Fuse
C4
FSOURCE IO Cell
Distance too large to meet V=IR drop

*Figure 3*

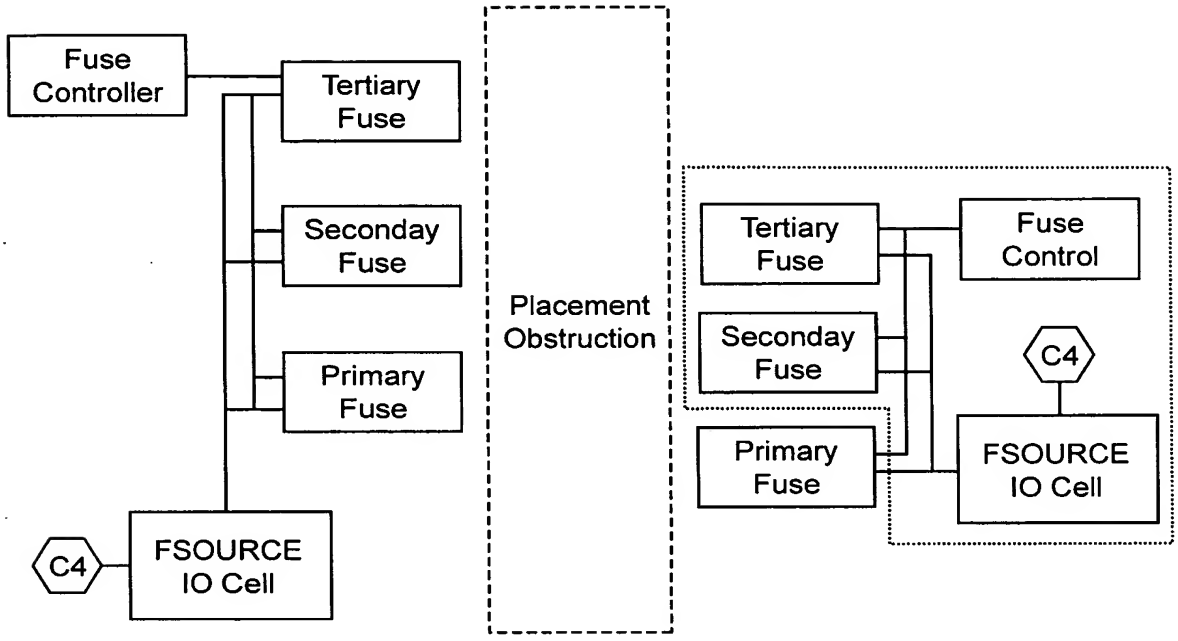
Fuse Controller
Tertiary Fuse
Seconday Fuse
Primary Fuse
C4
FSOURCE IO Cell
Placement Obstruction
Tertiary Fuse
Fuse Control
Seconday Fuse
C4
Primary Fuse
FSOURCE IO Cell

*Figure 4*

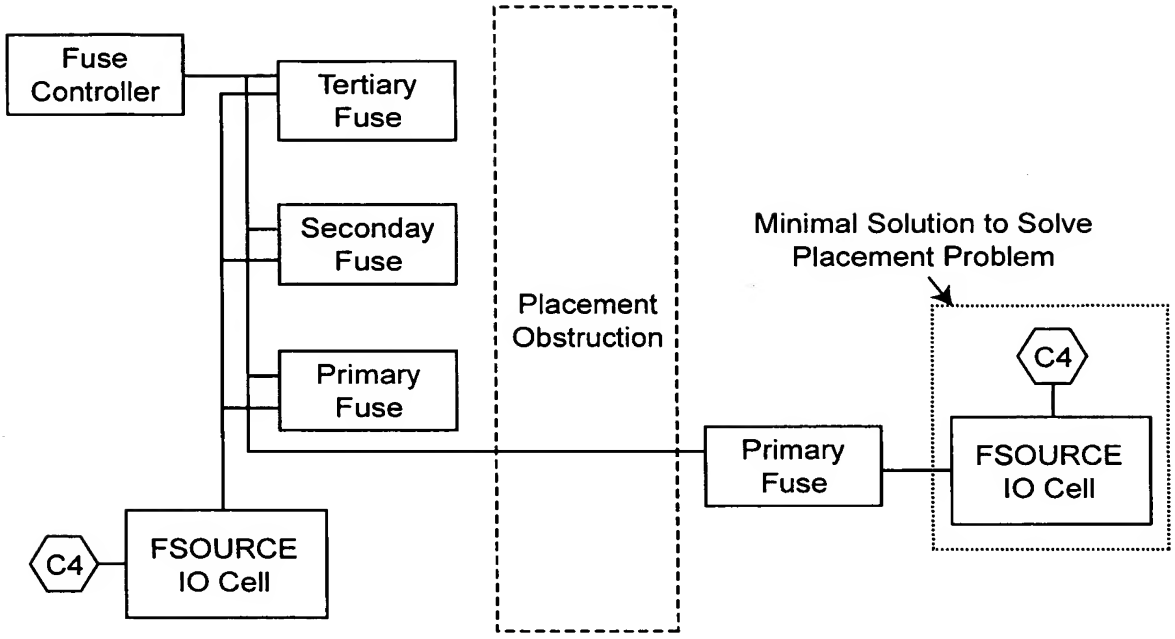
Fuse Controller
Tertiary Fuse
Seconday Fuse
Primary Fuse
C4
FSOURCE IO Cell
Placement Obstruction
Minimal Solution to Solve Placement Problem
Primary Fuse
C4
FSOURCE IO Cell

*Figure 5*

1. Determine P and N.

   P = number of primary fuse macros
   N = maximum allowable number of primary fuse macros per FSOURCE connection

2. Compare P and N and create FSOURCE C4s.

   If P<N, create one FSOURCE C4
   If P>N, create P/N (rounded up to nearest whole number) FSOURCE C4s

3. Divide primary fuse macros among FSOURCE C4s.

4. Floorplan the chip.

   If normal floorplanning constraints cannot be met, go on to step 5.

5. Increase number of FSOURCE C4s by one.

6. Divide primary fuse macros among FSOURCE C4s.

7. Repeat steps 4-6 until normal floorplanning constraints are met in Step 5.

*Figure 6*